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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,603	08/20/2003	Kazuyuki Yamada	9319S-000540	5576

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

Office Action Summary	Application No.	Applicant(s)	
	10/644,603	YAMADA ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/14/05 and 2/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/644603 Attorney's Docket #: 9319S-000540
Filing Date: 8/20/2003; claimed foreign priority to 7/15/2003 and 8/21/2002

Applicant: Yamada et al.

Examiner: Alexander Williams

Applicant's election with traverse of Species I of figure 3 (claims 9-15) filed 1/21/05 is acknowledged.

Applicant's arguments have been considered. If any non-elected species read on a generic allowed independent claim, upon allowance the independent claim, those particular claim will be examined at that time.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 1-8 and 16-23 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR ∋ 1.144 & MPEP ∋ 821.01).

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9 to 13 are rejected under 35 U.S.C. § 102(b) as being anticipated by Hatakeyama Tomoyuki (Japan Patent # 11-251363).

9. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show a semiconductor device mounting structure including a semiconductor device **1** having an electrode **3** and a substrate **5** having a wiring terminal **4** that is conductively connected to the electrode, wherein a width of one of the electrode and the wiring terminal is smaller than a width of the other of the electrode and the wiring terminal, and the one of the electrode and the wiring

terminal is embedded in a surface of the other of the electrode and the wiring terminal.
10. The semiconductor device mounting structure of claim 9, Tomoyuki show wherein a cross-sectional shape of the one of the electrode and the wiring terminal decreases towards the other of the electrode and the wiring terminal.
11. The semiconductor device mounting structure of claim 9, Tomoyuki show wherein the one of the electrode and the wiring terminal further comprises a material having a higher hardness than a hardness of the other of the electrode and the wiring terminal.
12. The semiconductor device mounting structure of claim 9, Tomoyuki show wherein the electrode and the wiring terminal both include a plurality of members, and widths of all of the one of the electrode and wiring terminals which are conductively connected to the other of the electrode and the wiring terminal are substantially the same.
13. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show a semiconductor device mounting structure including a semiconductor device **1** having an electrode **3** and a substrate **5** having a wiring terminal **4** that is conductiveiy connected to the electrode, wherein a width of the wiring terminal is smaller than a width of the electrode, and the wiring terminal is embedded in a surface of the electrode.

Claims 9 to 13 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kurashima Yohei (Japan Patent # 2001-223243).
9. Yohei (figures 1 to 12) specifically figure 3 show a semiconductor device mounting structure including a semiconductor device **10** having an electrode **16** and a substrate **20** having a wiring terminal **22** that is conductively connected to the electrode **22**, wherein a width of one of the electrode and the

wiring terminal is smaller than a width of the other of the electrode and the wiring terminal, and the one of the electrode and the wiring terminal is embedded in a surface of the other of the electrode and the wiring terminal.

10. The semiconductor device mounting structure of claim 9, Yohei show wherein a cross-sectional shape of the one of the electrode and the wiring terminal decreases towards the other of the electrode and the wiring terminal.

11. The semiconductor device mounting structure of claim 9, Yohei show wherein the one of the electrode and the wiring terminal further comprises a material having a higher hardness than a hardness of the other of the electrode and the wiring terminal.

12. The semiconductor device mounting structure of claim 9, Yohei show wherein the electrode and the wiring terminal both include a plurality of members, and widths of all of the one of the electrode and wiring terminals which are conductively connected to the other of the electrode and the wiring terminal are substantially the same.

13. Yohei (figures 1 to 12) specifically figure 3 show a semiconductor device mounting structure including a semiconductor device **10** having an electrode and a substrate having a wiring terminal that is conductiveiy connected to the electrode, wherein a width of the wiring terminal is smaller than a width of the electrode, and the wiring terminal is embedded in a surface of the electrode.

Claims 14 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatakeyama Tomoyuki (Japan Patent # 11-251363) in view of Applicant's Prior Art figures 10 and 11.

14. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show an device comprising: an retaining substance **6**; a wiring substrate **10** including a wiring terminal **4**; and a semiconductor device **1** including an electrode **3** conductively connected to the wiring terminal; wherein: a width of one of the wiring terminal and the electrode is smaller than a width of the other of the wiring terminal and the electrode; and the one of the wiring terminal and the electrode is conductively connected to the other of the wiring terminal and the electrode in a state where the one is embedded in a surface of the other. Tomoyuki fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

15. Tomoyuki (figures 1 to 13) specifically figures 1 and 2 show a device comprising: a retaining substance **6**; a wiring substrate **10** including a wiring terminal **4** conductively connected; and a semiconductor device **1** including an electrode **3** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; and the wiring terminal is embedded in a surface of the electrode. Tomoyuki fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 discloses show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to modify Tomoyuki's device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Claims 14 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurashima Yohei (Japan Patent # 2001-223243) in view of Applicant's Prior Art figures 10 and 11.

14. Yohei (figures 1 to 12) specifically figure 3 show a device comprising: a retaining substance **27**; a wiring substrate **20** including a wiring terminal **22** conductively connected; and a semiconductor device **10** including an electrode **16** conductively connected to the wiring terminal; wherein: a width of one of the wiring terminal and the electrode is smaller than a width of the other of the wiring terminal and the electrode; and the one of the wiring terminal and the electrode is conductively connected to the other of the wiring terminal and the electrode in a state where the one is embedded in a surface of the other. Yohei fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.
15. Yohei (figures 1 to 12) specifically figure 3 show a device comprising: a retaining substance **27**; a wiring substrate **20** including a wiring terminal **22** conductively connected; and a semiconductor device **10** including an electrode **16** conductively connected to the wiring terminal; wherein: a width of the wiring terminal is smaller than a width of the electrode; and the wiring terminal is embedded in a surface of the electrode. Yohei fail to explicitly show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance.

Applicant's Prior Art figures 10 and 11 discloses show an electro-optical device comprising: an electro-optical panel retaining an electro-optical substance for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

Therefore, it would have been obvious to one of ordinary skill in the art to the teach of Applicant's Prior Art figures 10 and 11 to

modify Yohei's device for the purpose of enabling connection of a wiring board without the provision of soft material for lands of the board at mounting flip chip and moreover with a fine pitch.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,738,738,777,780,784,786,734,787,728,787,780, 29/837,740	4/17/05
Other Documentation: foreign patents and literature in 257/778,738,738,777,780,784,786,734,787,728,787,780, 29/837,740	4/17/05
Electronic data base(s): U.S. Patents EAST	4/17/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/17/05